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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/564,582	01/12/2006	Celine Juliette Detecheverry	NL03 0878 US1	3317

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EXAMINER	
BAISA, JOSELITO SASIS	

ART UNIT	PAPER NUMBER
2832	

NOTIFICATION DATE	DELIVERY MODE
01/26/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/564,582	DETECHEVERRY ET AL.	
	Examiner	Art Unit	
	JOSELITO BAISA	2832	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

In view of the Appeal Brief filed on 07 October 2008, PROSECUTION IS HEREBY REOPENED. A new Office Action is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5-7, 9 and 11-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ballantine et al. [6489663] in view of Minami [6730983].

Regarding claims 1 and 22, Ballantine discloses a substrate 12 having a first major surface, an inductive element 16 fabricated on the first major surface of the substrate 12, the inductive element 14b comprising at least one conductive line, a plurality of conducting vias (tilling) structures (30, 32) in at least one layer, wherein the plurality of conducting vias (tilling) structures (30, 32) are electrically connected together and arranged in a geometrical pattern so as to substantially inhibit an inducement of an image current in the conducting vias (tilling) structures by a current in the inductive element 16 [Col. 6, Lines 13-33, Figures 1 and 2].

Ballantine discloses the instant claimed invention discussed above except for the conducting vias mentioned as tilling structures.

Minami discloses studs 12 as dummy or tilling structures. Minami further disclose that the plurality of dummy structures arranged to improve manufacturability of semiconductor device [Col. 4, Lines 1-15, Figures 1and 2] and [Col. 2, Lines 1-20].

It would have been obvious to one having ordinary skill in the art at the time of the invention to use dummy structures as taught by Minami to the device of Ballantine.

The motivation would have been to suppress dishing due to CMP and maintain the Q-value of the inductor to a large value [Col. 4, Lines 5-15].

With respect to claim 22, the claim is rejected for reciting method/steps derived from the structure of the rejected claim 1 above.

Regarding claim 2, Minami discloses the tilling structures 12 being made from tilling structure material, wherein the plurality of tilling structures 12 are arranged in a pattern so that the amount of tilling structure material in an area closer to the inductive element (5, 7) is smaller

than the amount of tilling structure material in an area farther away from the inductive element (5, 7) [see Figures 1 and 2].

Regarding claim 3, Ballantine discloses the conducting vias structures (30, 32) are located at different layers, each layer being arranged in a geometrical pattern so as to substantially inhibit an inducement of an image current in the conducting vias structures by a current in the inductive element 16 [Col. 6, Lines 13-33, Figures 1 and 2].

Ballantine discloses the instant claimed invention discussed above except for the conducting vias be mentioned as tilling structures and the structures is determined by a desired pattern density of the semiconductor device for improving at least one of a process window of lithography, uniformity of Chemical Mechanical Polishing removal rate and integrity of low-k dielectrics.

Minami discloses studs 12 as dummy or tilling structures. Minami further disclose that the plurality of dummy structure is determined by a desired pattern density of the semiconductor device for improving uniformity of Chemical Mechanical Polishing removal rate [Col. 4, Lines 1-15, Figures 1and 2].

It would have been obvious to one having ordinary skill in the art at the time of the invention to use dummy structures as taught by Minami to the device of Ballantine.

The motivation would have been to suppress dishing due to CMP and maintain the Q-value of the inductor to a large value [Col. 4, Lines 5-15].

Regarding claim 5, Ballantine discloses the conducting vias (tilling) structures (30, 32) at different layers are electrically connected to each other [Col. 6, Lines 13-33, Figure 2].

Regarding claim 6, Ballantine discloses the conducting vias (tilling) structures (30, 32) are connected to a DC potential (through 26) [Col. 5, Lines 65-67, Figure 2].

Regarding claim 7, Ballantine discloses the conducting vias (tilling) structures (30, 32) are a plurality of slender elongate elements [Col. 5, Lines 65-67, Figure 1].

Regarding claim 9, Hiromoto discloses the tilling structures (8b, 5b) are locally oriented perpendicular to the at least one conductive line of the inductive element [Abstract, Figure 1b].

Regarding claim 11, Ballantine discloses a ground shield 26 for shielding the inductive element 16 from a further layer [Col. 5, Lines 65-67, Figure 2].

Regarding claim 12, Ballantine discloses the further layer is the substrate 12 [Col. 5, Lines 31-67, Figure 2].

Regarding claim 13, Ballantine discloses connection means electrically connecting the plurality of conducting vias (tilling) structures (30, 32) with the ground shield 26 without creating a conductive loop [Col. 5, Lines 31-67, Figure 2].

Regarding claim 14, Minami discloses the tilling structures 12 are formed in a region other than a region directly below the inductive element (5, 7) [Col. 4, Lines 1-15, Figures 1and 2].

Regarding claims 15 and 16, Ballantine discloses a passive element, which is a capacitive element [Col. 5, Lines 31-55].

Regarding claim 17, Ballantine discloses the capacitive element comprises two capacitor electrodes at least one of the capacitor electrodes being formed by a plurality of conducting vias (tilling) structures (30, 32) [Col. 5, Lines 31-60].

Regarding claim 18, Ballantine discloses a capacitor electrode formed by a plurality of conducting vias (tilling) structures (30, 32) leads to a metal or polysilicon region density in the inductor vicinity respecting the design rules of advanced IC technologies [Col. 5, Lines 17-30].

Regarding claim 19, Ballantine discloses one capacitor electrode of the capacitive element is formed by the ground shield 26 [Col. 5, Lines 16-55].

Regarding claim 20, Ballantine discloses the integration of the capacitive element with the inductive element 14b is optimized to respect the metal pattern density in advanced silicon technologies [Col. 5, Lines 16-55].

Regarding claim 21, Ballantine discloses the distance between the capacitive element and the inductive element 16 is large enough to avoid a dominant fringe coupling between them [Col. 5, Lines 16-65].

Claims 4, 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ballantine in view of Minami as applied to claim1 above, and further in view of Kuroda et al. [6693315].

Ballantine in view of Minami discloses the instant claimed invention discussed above except for the tilling structures are plurality of substantially triangular elements.

Kuroda discloses dummy structures are substantially triangular elements [Col. 17, Lines 33-39].

It would have been obvious to one having ordinary skill in the art at the time of the invention to use triangular shape dummy pattern as taught by Kuroda to the structure of Ballantine in view of Minami.

The motivation would have been to provide flatness of the member surface embedded regardless of the shape of the dummy pattern [Col. 14, Lines 40-45].

Regarding claim 10, Ballantine discloses the elements of the conducting vias (tilling) structures are locally oriented perpendicular to the at least one conductive line of the inductive element 16 [see Figure 1].

Regarding claim 4, Ballantine in view of Minami discloses the instant claimed invention discussed above including dummy patterns in different layers except for the geometrical pattern of tilling structures at two different layers is different in shape.

Kuroda discloses geometrical pattern of dummy structures can be of any shape [Col. 17, Lines 33-39].

It would have been obvious to one having ordinary skill in the art at the time of the invention to use dummy patterns of different shape as taught by Kuroda to the different layer of Ballantine in view of Minami.

The motivation would have been to provide flatness of the member surface embedded regardless of the shape of the dummy pattern [Col. 14, Lines 40-45].

Response to Arguments

Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joselito Baisa whose telephone number is (571) 272-7132. The examiner can normally be reached on M-F 5:30 am to 2:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Elvin Enad can be reached on (571) 272-1990. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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